Improvement of Voltage Linearity in High-κ MIM Capacitors Using HfO_2–SiO_2 Stacked Dielectric

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***Abstract*—It is demonstrated that the voltage coefficients of capacitance (VCC) in high-κ metal–insulator–metal (MIM) capacitors can be actively engineered and voltage linearity can be significantly improved maintaining high capacitance density, by using a stacked insulator structure of high-κ and SiO_2 dielectrics. A MIM capacitor with capacitance density of 6 fFμm^2 and quadratic VCC of only 14 ppm/V^2 has been demonstrated together with excellent frequency and temperature dependence (temperature coefficients of capacitance of 54 ppm °C) as well as low leakage current of less than 10 nA/cm^2 up to 4 V at 125 °C.**

***Index Terms*—Analog/mixed-signal ICs, high-κ dielectric, high-κ/SiO_2 stack, metal–insulator–metal (MIM) capacitor, voltage coefficient of capacitance (VCC).**

I. INTRODUCTION

HIGH-κ metal–insulator–metal (MIM) capacitors have recently been studied for RF and analog/mixed-signal (AMS) ICs [1]–[9], and promising results for RF bypass or decoupling capacitor applications have been reported [2]–[4]. However, a high degree of voltage nonlinearity remains as a major concern on their application for high-performance AMS ICs [5]–[9]. Quadratic voltage coefficient of capacitance (VCC) α, a critical factor for the dynamic range of analog circuits [1], [10], is known to be inversely proportional to dielectric thickness [8], [9]. Therefore, α and capacitance density are in a trade-off relationship. Until now, there has been no known solution to achieve a capacitance density of higher than 5 fF/μm^2 while keeping α value of less than 100 ppm/V^2, both of which are requirements by the year 2010 according to IRTS roadmap [1], [2], [5]–[9].

In this letter, we demonstrate that voltage linearity can be manipulated by the means of canceling out effect of two opposite signs of α in HfO_2/SiO_2 stack MIM capacitor.

Manuscript received April 21, 2004; revised June 2, 2004. The review of this letter was arranged by Editor K. De Meyer.

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Digital Object Identifier 10.1109/LED.2004.832785

II. PRINCIPLE AND DEVICE FABRICATION

The voltage linearity of MIM capacitors are expressed by the VCC obtained from a second order polynomial equation of $C(V) = C_0 \cdot (\alpha \cdot V^2 + \beta \cdot V + 1)$, where C_0 is the capacitance at zero bias, α and β represent the quadratic and linear VCC, respectively [10]. When the dielectric of MIM capacitor is a stack of two different materials, the capacitance-voltage relationship of the MIM capacitor can be expressed as follows:

$$C_{\rm stack}(V) = \frac{C_1(V_1) \cdot C_2(V_2)}{C_1(V_1) + C_2(V_2)} = C_0 \cdot (\alpha \cdot V^2 + \beta \cdot V + 1) \quad (1)$$

where $C_1(V_1) = C_{01} \cdot (\alpha_1 \cdot V_1^2 + \beta_1 \cdot V_1 + 1)$ and $C_2(V_2) = C_{02} \cdot (\alpha_2 \cdot V_2^2 + \beta_2 \cdot V_2 + 1)$, obtained from the two single-layer MIM capacitors. In this case, the shape of the capacitance–voltage (*C*–*V*) curve of the stacked dielectric MIM will be determined by the voltage divided between the two dielectrics. With the relationship between voltage drops across the two dielectrics and the equivalent oxide thickness (EOT) of the each dielectric layer being

$$V_1 = \delta_1 \cdot V,\ V_2 = \delta_2 \cdot V,\ \delta_1 = \frac{C_0}{C_{01}} = \frac{\rm EOT_1}{\rm EOT_{stack}} \text{ and } \delta_2 = 1 - \delta_1,$$

α and β of the stacked dielectric MIM capacitor in (1) can be approximated to

$$\alpha = \delta_1^3 \cdot \alpha_1 + \delta_2^3 \cdot \alpha_2, \quad \text{and} \quad \beta = \delta_1^2 \cdot \beta_1 + \delta_2^2 \cdot \beta_2. \quad (2)$$

If the voltage nonlinearity is mainly originated from the bulk properties of the dielectric, such as the change of dielectric permittivity with the voltage across the dielectrics [11], (2) implies that virtually zero VCC values are obtainable by optimizing δ_1 and δ_2 in case that the VCC of the two dielectrics have opposite signs. It is well known that SiO_2 MIM capacitors show negative parabolic curves in a *C*–*V* relationship, while high-κ MIM capacitors exhibit strong positive parabola probably due to high degree of electric field polarization and carrier injections [8].

In this letter, atomic layer deposition HfO_2 and plasma-enhanced chemical vapor deposition SiO_2 films are evaluated in stack structures between TaN electrodes. HfO_2–SiO_2 dielectric layers are deposited on top of TaN (50 nm)/Ta (100 nm) bottom electrodes, which are formed on 500-nm isolation oxide. Sputtered TaN (150 nm) layer is used as a top electrode. The areas of the capacitors are defined by patterning the top electrodes using conventional optical lithography and dry etching. The maximum processing temperature used in this work is 420 °C. The film

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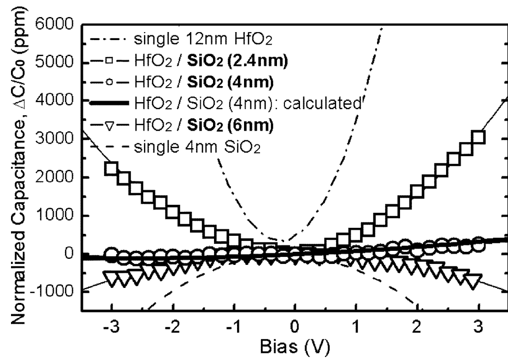

Fig. 1. Normalized *C–V* curves ($\Delta C/C_o$) of MIM capacitors with single HfO_2 (12 nm), single SiO_2 (4 nm), and HfO_2/SiO_2 stack. Capacitance was measured at 100 kHz. It shows that the voltage linearity of the stacked dielectric capacitors can be manipulated by changing the thickness ratio. The experimental (solid circles) and the calculated (solid grey line) $\Delta C/C_o$ curves of $HfO_2(12\ nm)/SiO_2(4\ nm)$ stack MIM capacitors are in excellent agreement.

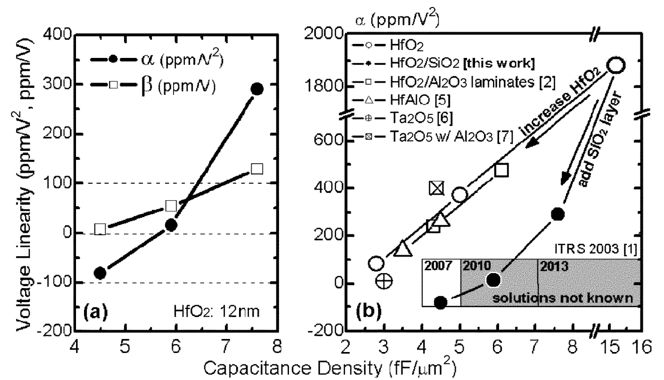

Fig. 2. (a) Trends of VCC values with respect to capacitance density when SiO_2 thickness changes from 6 to 2.4 nm at a given HfO_2 thickness of 12 nm. (b) Comparison with other high-κ MIM capacitors and the technology requirement for analog/mixed-signal capacitors specified by the latest ITRS.

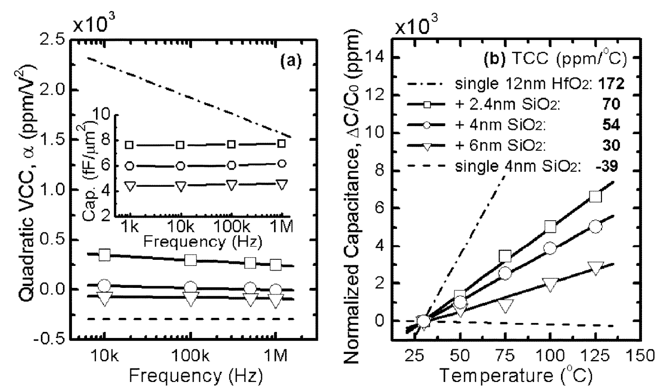

Fig. 3. (a) Frequency dependence of α and capacitance density of the HfO_2/SiO_2 stack MIM capacitors. (b) Adding SiO_2 layer improves TCC of HfO_2 MIM capacitors by the compensation effect due to negative TCC of SiO_2 MIM capacitors.

thicknesses are measured by cross-sectional transmission electron microscopy.

III. Results and Discussion

Fig. 1 shows the normalized *C–V* curves of MIM capacitors with single HfO_2 (12 nm), single SiO_2 (4 nm), and HfO_2/SiO_2 stack. In the stack MIM, the HfO_2 thickness is fixed at 12 nm while the SiO_2 thickness varies from 2.4 to 6 nm. The single HfO_2 capacitor shows a strong positive parabolic *C–V* curve, while the single SiO_2 capacitor shows a negative parabolic *C–V* curve. Adding SiO_2 layer to HfO_2 MIM capacitors significantly improves voltage linearity, which eventually becomes negative parabola when 6-nm-thick SiO_2 is used. This demonstrates that it is possible to engineer the quadratic VCC α to be virtually zero by modulating the HfO_2–SiO_2 thickness ratio. The solid grey line in Fig. 1 represents the calculated result obtained using (2) for the given thickness ratio. The excellent agreement between the experimental and the calculated results confirms that the improved voltage linearity of the HfO_2/SiO_2 stack MIM capacitors have resulted from the compensation of the opposite signs of VCC values between HfO_2 and SiO_2. Hence, (2) can be a tool to predict and optimize the *C–V* characteristics of any other stacked or sandwiched dielectrics MIM capacitors if VCC values of the single-layer MIM capacitors are given. VCC values as a function of capacitance density extracted from the *C–V* curves in Fig. 1 are plotted in Fig. 2(a). In this case, the curve of α crosses the zero line at the capacitance density of about 5.8 fF/μm^2, which is high enough for the AMS IC requirement by year 2010 [1]. By inserting SiO_2 into high-κ MIM capacitor, total capacitance density decreases. As seen in Fig. 2(b), however, adding SiO_2 results in a faster drop in α, compared to scaling thickness of HfO_2 because of the canceling out effect of α due to the negative signed α of SiO_2. In Fig. 2(b), most recent results on high-κ materials, such as HfO_2/Al_2O_3 laminates [2], HfAlO [5], single layer Ta_2O_5 [6], and Ta_2O_5 with Al_2O_3 barriers [7], are compared together. In our experiment, the best result was obtained from the $HfO_2(12\ nm)/SiO_2(4\ nm)$ stack with its quadratic VCC and capacitance density of 14 ppm/V^2 and 6 fF/μm^2, respectively. These data fall well within the *solutions-not-known* region in Fig. 2(b) according to the International Technology Roadmap for Semiconductors [1]. The optimum ratio of the dielectric thickness can vary with temperature, as the α value tends to increase with temperature. Therefore, in actual device design, it is advisable to optimize the ratio of the dielectric thickness considering the α value at the highest operating temperature required, so that the VCC requirement is to be met over the entire operating temperature.

Fig. 3(a) shows the frequency stability of α in HfO_2–SiO_2 stack MIM capacitors and single HfO_2 MIM capacitor. The single HfO_2 MIM has strong dependence of α on frequency, which is undesirable but a common property of high-κ MIM capacitors [2]. However, the HfO_2–SiO_2 stack MIM capacitors show highly stable α value with frequency, probably due to nondispersive characteristic of SiO_2. The compensation effect using the stack layer is also found in temperature coefficients of capacitance (TCC), which is another important parameter for precision MIM capacitors. Fig. 3(b) clearly shows the canceling out between strong positive values of TCC in HfO_2 and well known negative TCC in SiO_2 [12]. The MIM capacitors with 4- and 6–nm SiO_2 layers show the TCC values of 54 and 30 ppm/°C, respectively, which are comparable to those reported for 90-nm RF/AMS foundry technology [13], but have three times higher capacitance density.

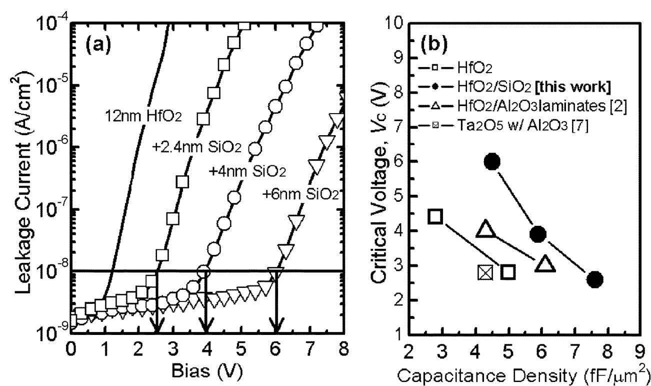

Fig. 4. (a) Leakage current versus voltage for the HfO_2–SiO_2 stack MIM capacitors. (b) Critical voltage, V_c, versus capacitance density. The V_c values are obtained from the high temperature (125 °C). For the same capacitance density, V_c of HfO_2–SiO_2 stack is even higher than that of other high-κ MIM capacitors.

The added thin SiO_2 layer plays a critical role in leakage current $(J_{\rm leak})$ as well. Fig. 4(a) shows that increasing the thickness of SiO_2 layer substantially delays the on-set of the Poole-Frenkel type conduction [2], [3]. Although relatively thin HfO_2 and SiO_2 films are used to obtain high capacitance density, $J_{\rm leak}$ of less than 10 nA/cm^2 at $\pm$3.3 V, 125 °C is obtained, and the critical voltage V_c, the bias which keeps $J_{\rm leak}$ less than the required 10 nA/cm^2, of higher than $+4$ V is achieved from the capacitors with 4- and 6-nm SiO_2 layers. The result also indicates that the SiO_2 layer thickness must not be in direct tunneling regime in order to ensure V_c to be higher than $\pm$3.3 V. Even higher V_c and lower $J_{\rm leak}$ are obtained under negative bias at top electrode (data not shown here). This asymmetry is due to asymmetric energy band diagram of metal–HfO_2–SiO_2–metal structure [14]. Compared to other high-κ MIM capacitors, Fig. 4(b) shows that HfO_2–SiO_2 stack has higher V_c at a given capacitance density, which may be attributed to the wide bandgap and low defect density of SiO_2 layer.

IV. Conclusion

We demonstrated that a well-engineered HfO_2–SiO_2 stacked dielectric MIM capacitor can achieve a high capacitance of 6 fF/μm^2 together with a small quadratic VCC α of 14 ppm/V^2, which is the best ever reported so far. It also showed good TCC value of 54 $\mathrm{ppm}/^\circ$C and low leakage current less than 10 $\mathrm{nA/cm^2}$ at 125 °C. The results suggest high-κ/SiO_2 MIM capacitor to be an excellent candidate for future AMS IC applications.

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